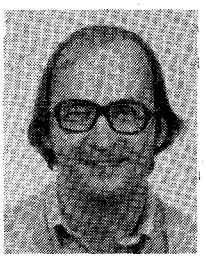

Gheorghe Smarandoiu (S'74-M'76) was born in Brasov, Romania, on June 18, 1946. He received the electronic engineer degree from the Institutul Politehnic Bucuresti, Bucharest, Romania, in 1969, the M.Eng degree in 1975 and the D.Eng. degree in 1978 both from the University of California, Berkeley.

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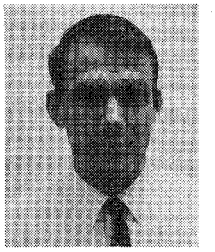
David A. Hodges (S'59-M'65-SM'71-F'77), for photograph and biography, see page 294 of the June 1978 issue of this JOURNAL.

Paul R. Gray (S'65-M'69-SM'76), for photograph and biography, see page 294 of the June 1978 issue of this JOURNAL.



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He joined Bell Laboratories, Naperville, IL, in 1966 where his primary work was involved exploratory development of an optical memory system, using holographic storage. After a period with Siliconix, Inc., Santa Clara, CA, where his primary work was on data conversion and telecommunication devices, he joined Silicon Systems, Inc., Irvine, CA, in January 1978.

Mr. Landsburg is a member of Phi Eta Sigma, Tau Beta Pi, Eta Kappa Nu, Phi Kappa Phi, and Delta Mu Delta.

An Automatic *C-V* Plotter and Junction Parameter Measurements of MIS Schottky Barrier Diodes

JUH TZENG LUE

Abstract—**An automatic *C-V* plotter which employs phase-locked loop integrated circuits to sense the in-phase and quadrature-phase current signal passing through the diode under test is described. The output voltage at a moderately high frequency is directly proportional to the junction capacitance of the diode when the reference signal of the phase detector is in phase with the input signal. The junction resistance of the diode can be simultaneously determined by measuring the quadrature-phase signal. This instrument has successfully measured the *C-V* characteristics of Schottky barrier solar cells.**

I. INTRODUCTION

THE capacitance measurement using point by point plotting of *C-V* bridge data is always tedious and laborious. For rapid accessment of devices, an automatic *C-V* plotter is highly desirable. To determine surface states and barrier heights for MIS (metal-insulator-semiconductor) Schottky barrier solar cells, a rapid *C-V* measurement is urgently required, since the surface states depend on the bias sweeping time and charge storage history.

The high frequency capacitance technique developed by Terman [1] to determine the surface-state density requires a graphical differentiation of the experimental *C-V* data compared with an ideal *C-V* curve, which is hard to determine accurately. Furthermore, the surface charging time is much longer than the period of the test frequency. The ac conductance technique employed by Nicollian and Goetzberger [2], which yields accurate information about surface states, suffers from the disadvantage that the admittance due to capacitive and resistive components are not distinguishable. The quasi-static technique for MOS *C-V* measurement [3], based on a measurement of the MOS charging current in response to a linear voltage ramp, is not able to measure MIS solar cells where the insulating layer is so thin that the current can directly tunnel through.

The current sensing circuit reported recently by Forward *et al.* [4] which measures the in-phase signal, gives a simple and direct readout of the *C-V* relationships. This method though is unable to measure the out of the phase signal which can predict other parameters of the diode.

In this work an automatic *C-V* plotter is described which employs phase-locked loop integrated circuits to sense the in-phase and quadrature-phase current signal passing through the capacitor under test. The output voltage at a moderate frequency is proportional to the junction capacitance of the diode when the reference signal of the phase detector is in phase with the input signal. The junction resistance of the diode can be simultaneously determined by measuring the quadrature-phase signal. Therefore, the junction parameters of the diode can be accurately determined by a fairly simple method with an instrument that can be easily constructed by using readily obtainable FM demodulating components.

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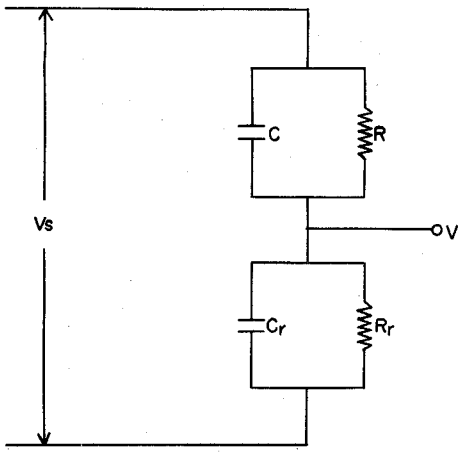

Fig. 1. Diode equivalent circuit and measuring functions.

II. Operational Principles

With the applied signal at an intermediate frequency, the series resistance is negligibly smaller than the reactance of the diode. By an inspection of Fig. 1, where R and C represent the junction resistance and capacitance of the diode, the output voltage which is in phase with the input signal can be written as

$$V_{0^\circ} = \frac{[1 + \omega^2 RC(C + C_r)R]\ V_s}{1 - \omega^2(C + C_r)^2 R^2}. \tag{1}$$

This equation can be simplified as

$$V_{0^\circ} \approx \frac{C}{C_r} V_s, \tag{2}$$

if $\omega(C + C_r)R \gg 1$ and $C \ll C_r$. Therefore, the in-phase output voltage is directly proportional to the junction capacitance and is independent of the test frequency.

The quadrature-phase output voltage is

$$V_{\pi/2} = \frac{\omega RC - \omega(C + C_r)R}{1 - \omega^2(C + C_r)R^2} V_s. \tag{3}$$

The junction resistance R is approximately equal to

$$R = \frac{1}{\omega C} \frac{V_{0^\circ}}{V_{\pi/2}}, \tag{4}$$

providing that the same conditions as in (2) are applied. A resistor R_r is placed in parallel with C_r so that the bias can be applied to the diode. But the conditions, i.e., $R_r \gg 1/\omega C$ and $R_r \ll R$ should be satisfied in order not to introduce extra errors. For example, if $C_r = 0.1\ \mu$F, $C \sim 1000$ pF for a typical MIS solar cell, a value of $R_r = 10\ \text{M}\Omega$, $\omega = 10$ kHz will yield an accuracy of the determination of the capacitance within 3 percent.

A phase-locked loop integrated circuit, when operated as a demodulator, may be thought of as a coherent detector [5]. There are two conflicting requirements on loop bandwidth:

1) loop bandwidth must be as narrow as possible to minimize output phase jitter due to external noise;

2) the loop bandwidth should be made as large as possible to minimize transient error due to signal modulation, output jitter due to internal oscillator (VCO) noise, and to obtain best tracking and acquisition properties.

These two conflicting conditions can be solved by using two phase-locked loops. One with large time constant (narrow bandwidth) is used to obtain higher loop gain and lower noise jitter for the phase detector, and another one with wide bandwidth is used to increase the damping factor and to improve the stability of the VCO.

The phase of the reference square wave from the VCO can be shifted continuously from 0° to 90° with the aid of an external potentiometer and a proper value of the charging capacitor. The peak phase error in the loop is equal to

$$\theta = \eta \frac{\Delta\omega}{\omega_n},$$

where η is the damping factor, ω_n is the natural frequency, and $\Delta\omega$ is the frequency range to be explored. The η and ω_n have been derived as [5]

$$\eta = \frac{1}{2}\left[\frac{k_o k_D}{(R_1 + R_2)C_1}\right]^{1/2}\left[R_2 C_1 + \frac{1}{k_o k_D}\right], \tag{5}$$

$$\omega_n = \left[\frac{k_o k_D}{(R_1 + R_2)C_1}\right]^{1/2}$$

where the parameter k_o, k_D, R_1, R_2, and C_1 can be readily realized from Fig. 2. Thus θ is given by the expression

$$\theta \approx \frac{\Delta\omega\left[R_2 C_1 + \dfrac{1}{k_o k_D}\right]}{2}.$$

The greater the time constant $R_2 C_1$ the larger the peak phase error, and the more difficult it is to synchronize with the input frequency.

The block diagram of the measuring system is shown in Fig. 3. The potentiometer R_1 attenuates the input signal to a voltage sufficiently small so as not to distort the linearity of the phase detector while maintaining a large enough signal to the input of the phase detector. Similar phase-locked loops are used for phase detector and phase shifter, respectively. The phase relationship between the input signal and the reference voltage is checked by a dual-trace oscilloscope.

III. Circuit Description

The circuit detail is shown in Fig. 4. The phase of the square wave output from IC_2 can be shifted continuously from 0° to 90° by adjustment of R_3 provided that the charging capacitor C_3 has been properly chosen at a given frequency. Since the output at pin 7 of IC_1 has a floating dc level of 4 V accompanying the 1 V ac signal, a clamping of this dc level in order not to saturate the following dc amplifier is necessarily. The Zener diode D_2 can do this job easily.

A linear ramp generator constructed using a simple linear integrated circuit, as shown in Fig. 5, is used to bias the diode. When the transistor Q_1 is reverse biased in the cutoff region, the small reverse collector saturation current I_{CBO} corresponds to a constant current to charge the condenser of the integrating circuit. The value of I_{CBO} extends over a very large range

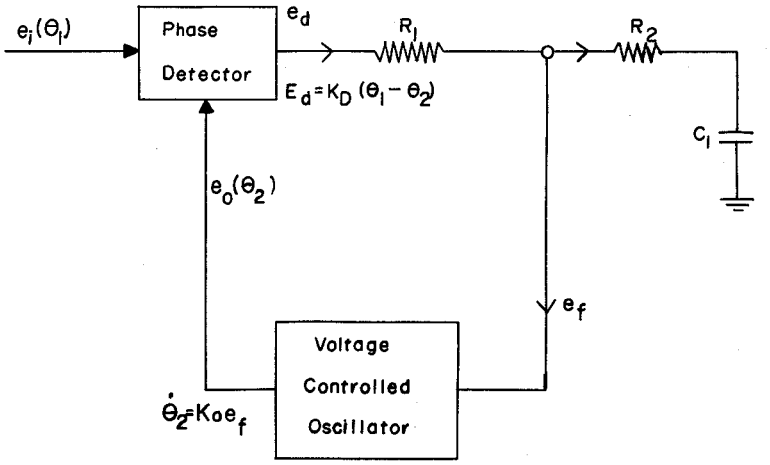

Fig. 2. Block diagram showing the function of the phase-locked loop integrated circuit.

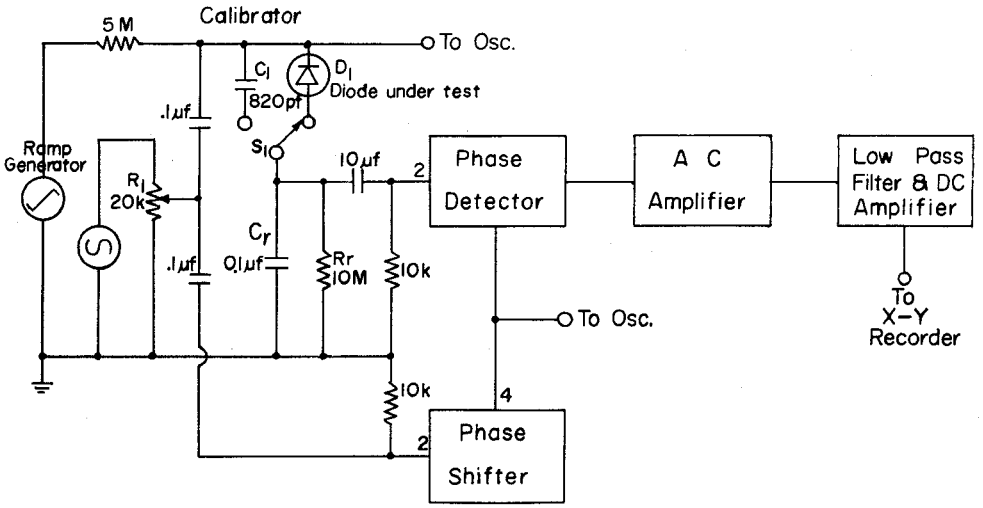

Fig. 3. Block diagram of the *C-V* measuring system.

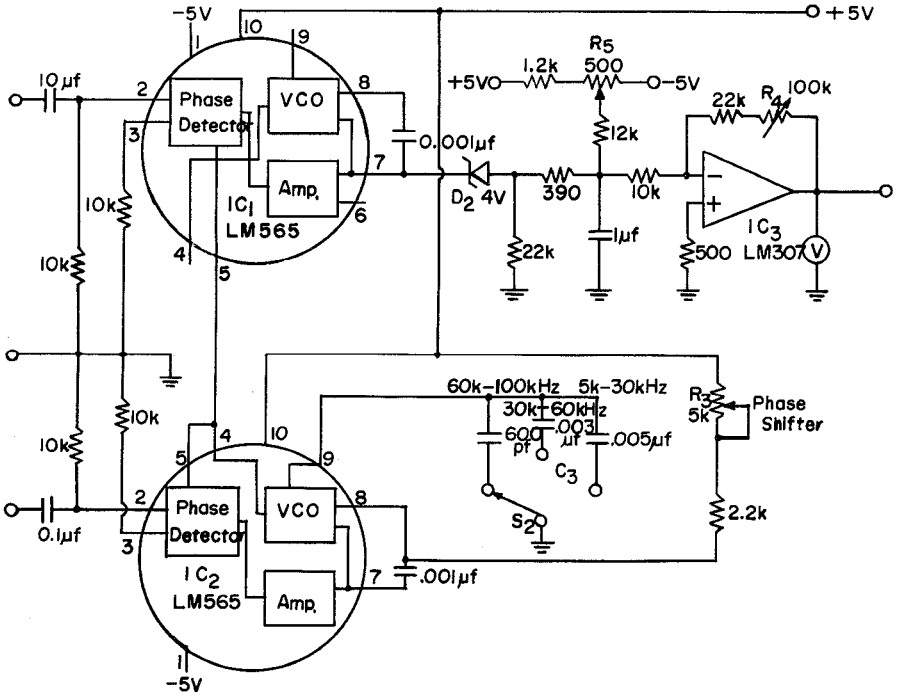

Fig. 4. Circuit detail of the phase detector and phase shifter.

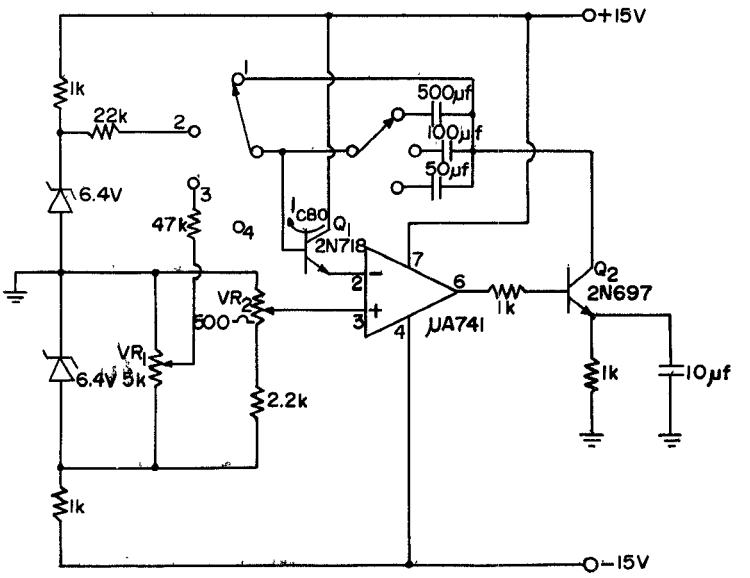

Fig. 5. Circuit detail of a linear ramp generator. VR_1: sweep rate control; VR_2: zero offset (+0.35 V → −0.8 V); switch position: 1) off, 2) ramp down, 3) ramp up, 4) standby.

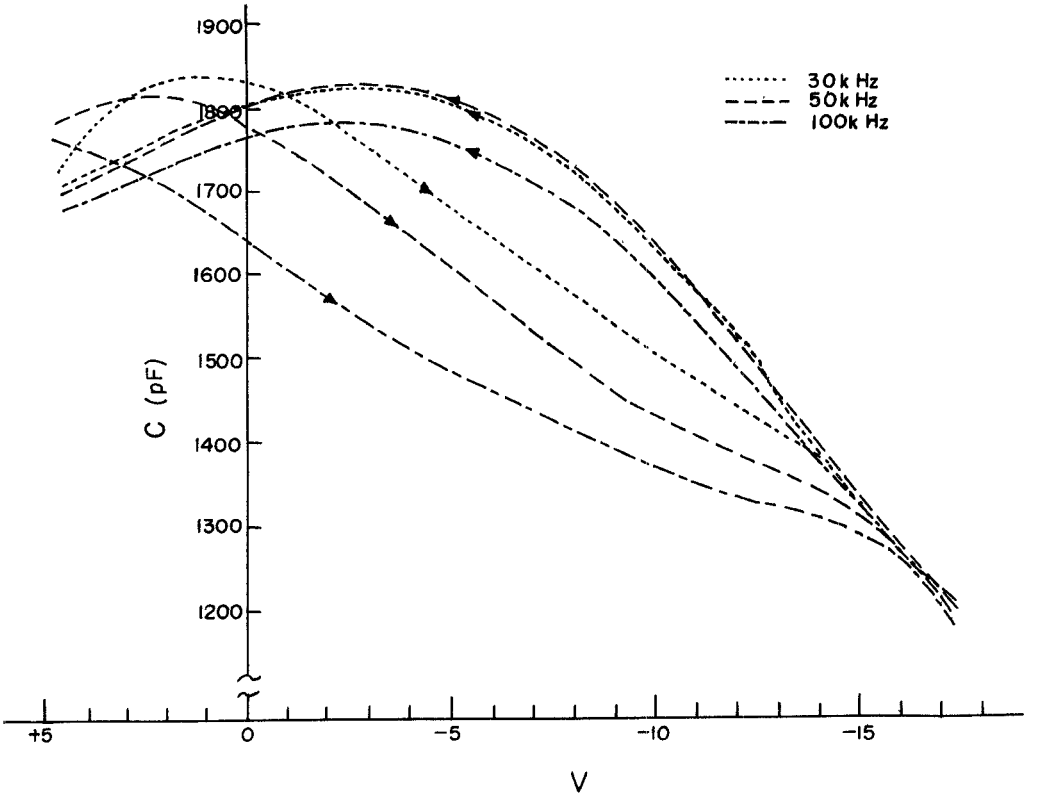

Fig. 6. C-V plot of a Schottky barrier solar cell. Sweep rate: 0.2 V/s up, 0.3 V/s down.

from several nanoamperes to microamperes depending on the reverse biasing condition, which is controlled by VR_1 and the sweeping rate. The sweeping up and down rate can be varied from ±10 mV/s to ±1 V/s.

IV. Performance

For a quick measurement of diode junction parameters the following procedures are suggested:

1) with the input signal attenuated to zero, the dc output at IC_3 should be zero; if not, adjust the reference level R_5;

2) adjust the resistor R_1 so that the input signal across D_1 or C_1 is below 0.2 V;

3) vary the potentiometer R_3 to see that the reference square wave from the output of VCO (pin 4 of IC_2) can be synchronized with the input signal, and its phase can be shifted from 0° to 90°; if not, change the charging capacitor C_3;

4) using an oscilloscope, adjust the phase shifter R_3, to see that the signal applied to the diode (or the calibrating capacitor C_1) is in phase with the reference signal from the VCO of IC_2;

5) adjust the gain control R_4, so that the dc output voltage has the same reading as the value of the calibrating capacitor;

6) when S_1 is switched into the test diode, the dc output reading indicates the value of the junction capacitance of the diode.

An automatic C-V plot for a Schottky barrier solar cell fabricated with a p-type, 1 $\Omega \cdot$ cm [1] silicon wafer with an interface oxide layer of 24 Å and an active area of 0.36 cm^2 is shown in Fig. 6. The MIS capacitance is composed of two components connected in series. The first capacitance is the oxide capacitance which is independent of the applied voltage, while the second is the capacitance of the silicon surface due to the space-charge region. The space-charge region is named "accumulation", "depletion", and "inversion" for forward, reverse, and strong reverse bias, respectively. With increasing applied voltage (both for forward and reverse bias), the space-charge region widens, resulting in a decrease in the space-charge capacitance and its accompanied total capacitance.

The MIS characteristics will be affected by the presence of the surface states. The total charging current to the surface of the silicon will be the sum of two components, one which goes to charging the depletion region in the silicon, and the other one which goes to charging the surface state. The surface states have a charging time constant τ. At low frequencies where $\omega\tau << 1$, all the surface states can be affected by the applied field and the surface-state capacitance appears directly in parallel with the depletion capacitance, resulting in a higher value of total capacitance. At high frequencies where $\omega\tau >> 1$, the surface state cannot respond to the input signal and the surface-state capacitance gives no contribution to the total capacitance. In general, the capacitance of the device will decrease monotonically with increasing frequency at a given bias voltage. The decrease of total capacitance with increasing frequency and bias voltage, as shown in Fig. 6, has been reported by Terman [1].

The hysteresis property of the C-V plots comes from the charging and discharging of the surface states and is a function not only of bias voltage but also of sweep rate. The discrepancy of the measured capacitance between the up and down sweep can be greatly reduced by annealing the device in hydrogen gas at a temperature of 300°C for one hour before each sweep. A similar hysteresis effect has been observed by Forward *et al.* [4].

To measure the junction resistance R, the reference phase is shifted $\pi/2$ of the input signal. The dc output voltage is then the reading of $V_{\pi/2}$, and R can be calculated directly via (4).

This instrument can be economically constructed from readily obtainable commercialized FM demodulators and can accurately determine the junction parameters of diodes.

Acknowledgment

The author is indebted to S. P. Lee for his construction of the slow sweep ramp generator.

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